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Comparative studies on switched capacitor based single phase multilevel inverter fed from PV systems for isolated applications

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ABSTRACT

This paper presents comparative studies on different levels of single phase inverter for standalone photo voltaic systems with simple pulse width modulation scheme. The pulse width modulation scheme utilizes one triangular carrier signal and multi sinusoidal reference signal for controlling the switches of the inverter. The performance of the five and seven level inverter has been verified through MATLAB simulation results. The simulation results prove that, the seven level inverter provides more fundamental rms output voltage and less total harmonic distortion in the inverter output voltage without using passive filter than conventional two level inverter.

Keywords: Multilevel inverter, photovoltaic (PV) system, pulse width-modulated (PWM), Total Harmonic Distortion (THD).

1. INTRODUCTION

Nowadays, power electronic researchers are concentrating in the field of alternative energy sources due to the constantly growing energy demand and the rapid depletion of fossil-fuel reserves. The fuel of renewable energy source being derived from natural and available resources is expected to capable of supplying humanity energy for almost 1billion years. Renewable energy sources would also reduce environmental pollution such as; air pollution caused by booming of fossil fuels. One of the most popular renewable energy source is Photovoltaic generation system. The generated energy from the photovoltaic system can be delivered to the power network and also in isolated applications.

Normal operation of CSI and VSIs can be classified as two level inverters because, the power switches connected to either positive or the negative DC bus. If more than two voltage levels were available to the inverter output terminals, the AC output terminals, the AC output could better approximate a sine wave. For this reason, multilevel inverters are preferred than two level inverter because it provides more fundamental output voltage with reduced harmonic spectrum in the inverter output. The concept of multilevel inverter is kind of modification of two level inverter. In order to create a smoother stepped output waveform, more than two voltage levels are combined together and the output waveform obtained. It has lower dv/dt and lower harmonic distortions and smoothness of the waveform is proportional to the voltage levels, as increase the voltage level the waveform becomes smoother.

Several topologies of multilevel inverters are reported in several literatures. The basic topologies of multilevel inverters are diode clamped, flying capacitor, cascaded H-bridge multilevel inverter. An m level Diode clamped inverter requires (2m - 2) power switching devices, (m -1) input voltage source and (m-1)(m-2) diodes in order to produce m level output voltage. The drawback of Diode clamped multilevel inverter is difficult, because of quadratic relation between number of diode and number of level especially, when number of level is higher and also it becomes stressful to maintain charging and discharging cycle. The configuration of flying capacitor multilevel inverter topology is quite similar to Diode clamped multilevel inverter topology except the difference that flying capacitor is used in order to obtain the voltage levels instead of diodes. An m level flying capacitor multilevel inverter needs (2m-2) power switches and (m-1) number of capacitors to obtain m level inverter output voltage. The drawback of flying capacitor multilevel inverter is difficult to recharge and voltage control is difficult for all the capacitors. In the case of Cascaded H – bridge multilevel inverter, each separate DC source is connected at each H bridge module. Each inverter level can generate different voltage outputs by connecting the DC source to the AC output by different combinations of the switches. If there are m cells in H – bridge multilevel inverter of output voltage level will be (2m+1). This type of inverter has advantage over the other two as it requires less number of components as compared to other two types of inverters and so its overall weight and price is also less. The drawback of this type of type of multilevel inverter is every H-Bridge needs separate source. Unequal voltage may be appeared because of using separate dc source.

This paper describes the comparison of novel modified H- bridge single phase single source multilevel inverter with five level and seven level inverter performance has been analyzed with simple pulse width modulated (PWM) scheme in detail.

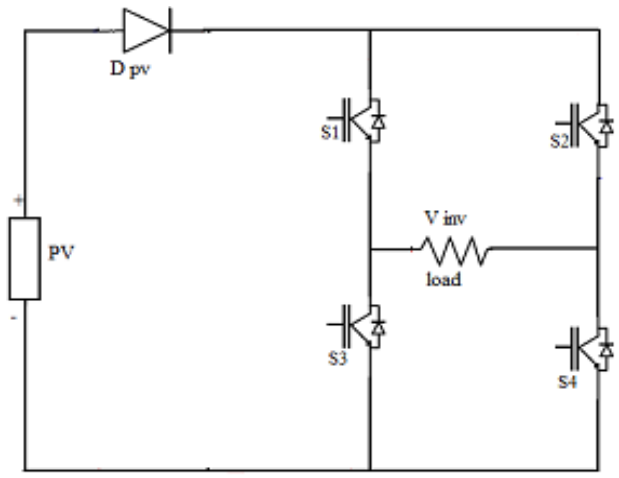


Figure 1 Single-phase H-bridge conventional two-level inverter topology

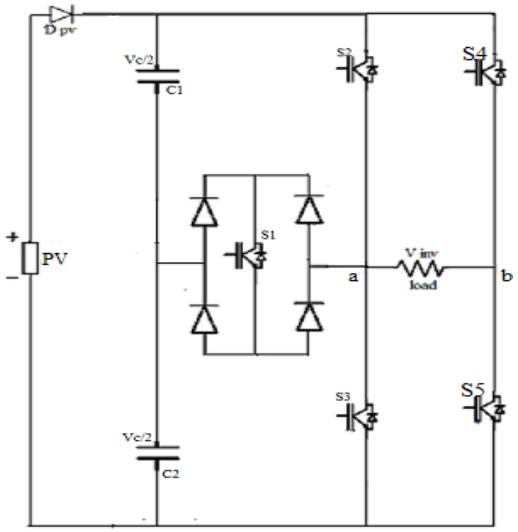


Figure 2 Single-phase single DC source five-level inverter topology

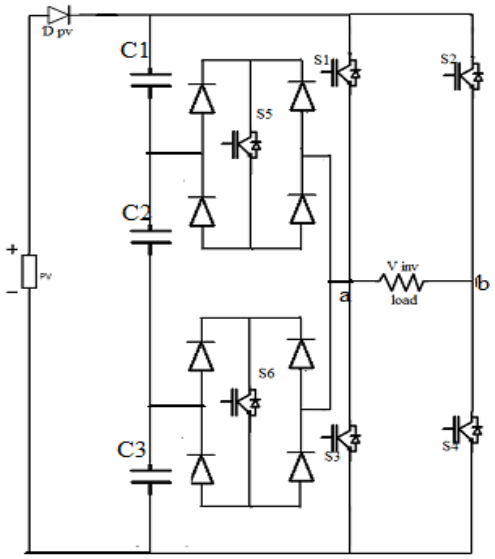
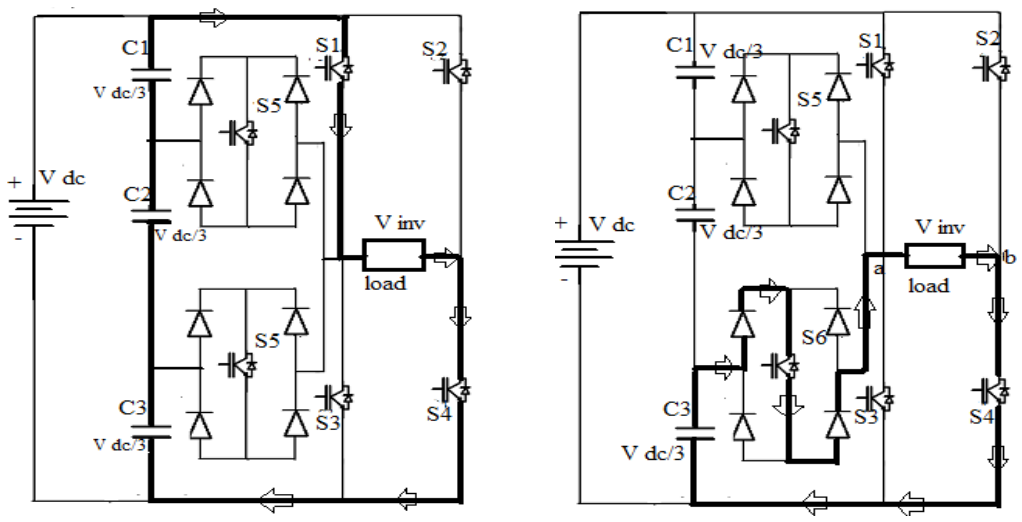


Figure 3 Single-phase seven-level inverter topology



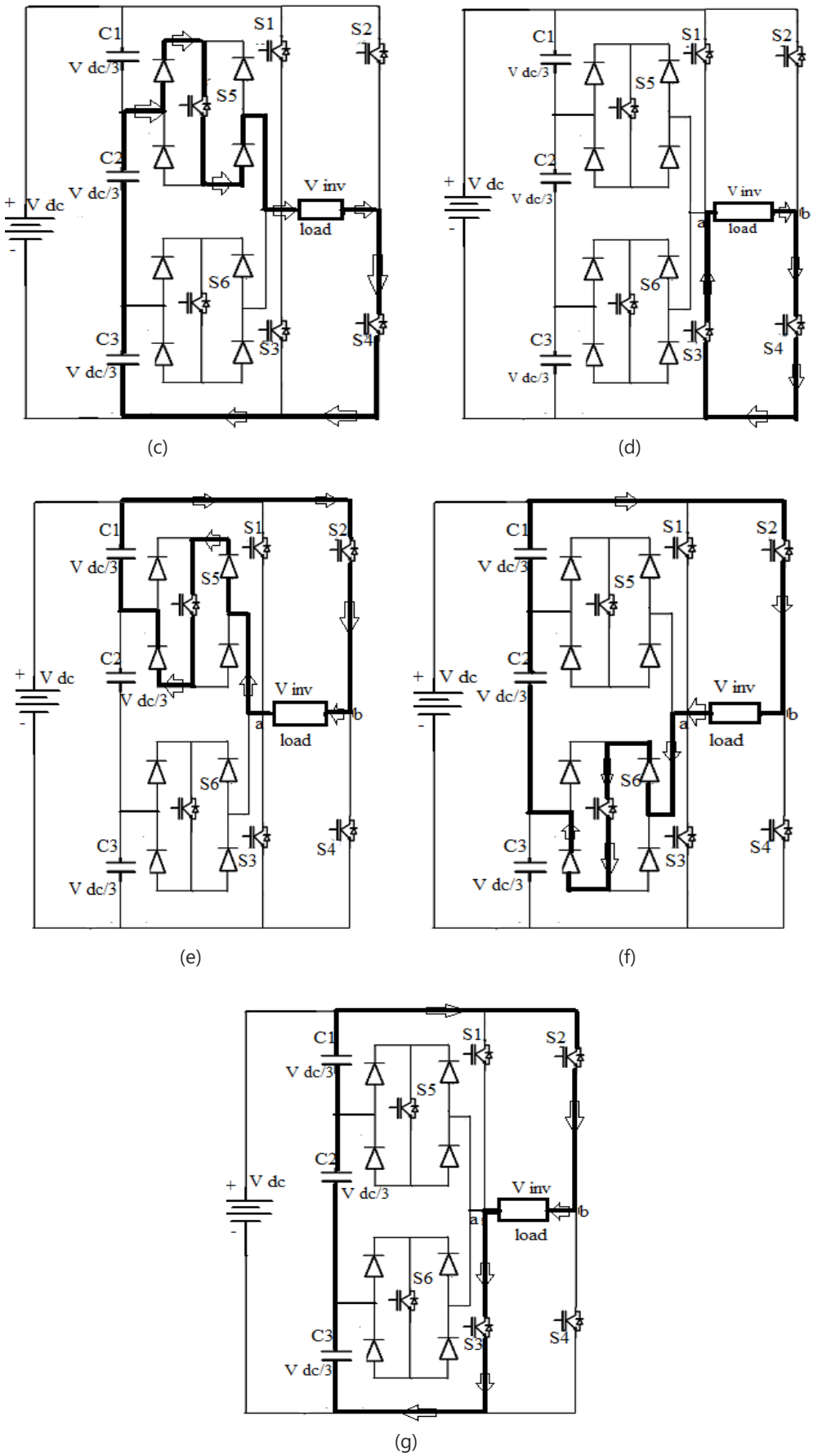


Figure 4 Switching sequence required to generate the output voltage
(a)$V_{inv}=V_{dc}$ (b)$V_{inv}=V_{dc}/3$ (c)$V_{inv}=2V_{dc}/3$ (d)$V_{inv}=0$ (e)$V_{inv}= -V_{dc}/3$ (f)$V_{inv}= -2V_{dc}/3$ (g)$V_{inv}= -V_{dc}$

2. SEVEN LEVEL MULTILEVEL INVERTER TOPOLOGY

The seven level single-phase single dc sourced inverter is consists of single-phase conventional H-bridge inverter, two bidirectional switches and a capacitor voltage divider network of C_1, C_2, and C_3. The H-bridge inverter topology has lot of advantageous over diode clamped and flying capacitor multilevel inverter topologies, it requires less number of components for inverters of the same number of levels and so its overall weight and price is also less. Photovoltaic arrays were connected to the multilevel inverter. The power generated by the multilevel inverter is to be delivered to the isolated load. Seven output voltage levels can be produced by proposed switching of the multilevel inverter from the single dc supply voltage. The output voltage levels are V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$,$-2V_{dc}/3$, $-V_{dc}/3$.

Table 1 Output voltage according to the switches ON-OFF condition for seven-level inverter

Inverter Output Voltage (Vo)	**Switching State Combination**					
	S_1	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**
V_{dc}	1	0	0	1	0	0
$2V_{dc}/3$	0	0	0	1	1	0
$V_{dc}/3$	0	0	0	1	0	1
0	0	0	1	1	0	0
	1	1	0	0	0	0
$-V_{dc}/3$	0	1	0	0	1	0
$-2V_{dc}/3$	0	1	0	0	0	1
$-V_{dc}$	0	1	1	0	0	0

Table 1 shows that the switching sequences to generate the seven levels of output voltage (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$,$-2V_{dc}/3$, $-V_{dc}$).

Mode 1: Maximum positive output voltage ($+V_{dc}$)

In this mode of operation, the switches S_1 and S_4 conduct. During this period, the current flows from switch S_1, load and S_4. When switch S_1 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is $+V_{dc}$. Fig.4.(a) shows the current path of this mode.

Mode 2: Two-third positive output voltage ($+2V_{dc}/3$)

In this mode, the bidirectional switch S_5 and S_4 conducts. During this period, the current flows from bidirectional switch S_5, load and switch S_4. When the bidirectional switch S_5 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is ($+2V_{dc}$ /3). Fig 4. (b) shows the current path of this mode.

Mode 3: One-third positive output voltage ($+V_{dc}$ /3)

In this mode, the bidirectional switch S_6 and S_4 conducts. During this period, the current flows from bidirectional switch S_6, load and switch S_4. When the bidirectional switch S_6 is ON, the load positive terminal connecting to V_{dc} and when switch S_4 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is ($+V_{dc}$ /3). Fig 4. (c) Shows the current path of this mode.

Mode 4: Zero output voltage (0 V_{dc})

This mode voltage can be produced by two combinations of switching. In this mode, the switches S_3 and S_4 conducts or S_1 and S_2 conducts, and the remaining switches are in OFF condition; the load terminal (a and b) is short circuit, the voltage between the load terminal is zero. Fig 4.(d) shows the current path of this mode.

Mode 5: One-third negative output voltage (-V_{dc} /3)
In this mode, the bidirectional switch S_5 and S_2 conducts. During this period, the current flows from bidirectional switch S_5, load and switch S_2. When the bidirectional switch S_5 is ON, the load positive terminal and when switch S_2 is ON, the load negative terminal connecting to V_{dc}. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is (-V_{dc} /3). Fig 4.(e) shows the current path of this mode.

Mode 6: Two-third negative output voltage (-2V_{dc}/3)
In this mode, the bidirectional switch S_6 and S_2 conducts. During this period, the current flows from bidirectional switch S_6, load and switch S_2. When the bidirectional switch S_6 is ON, the load positive terminal and when switch S_2 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is (-2V_{dc} /3). Fig 4.(f) shows the current path of this mode.

Mode 7: Maximum negative output voltage (-V_{dc})
In this mode, the switches S_2 and S_3 conduct. During this period, the current flows from switch S_2, load and S_3. When switch S_2 is ON, the load negative terminal connecting to V_{dc} and when switch S_3 is ON, the load positive terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is -V_{dc}. Fig 4(g) shows the current path of this mode.

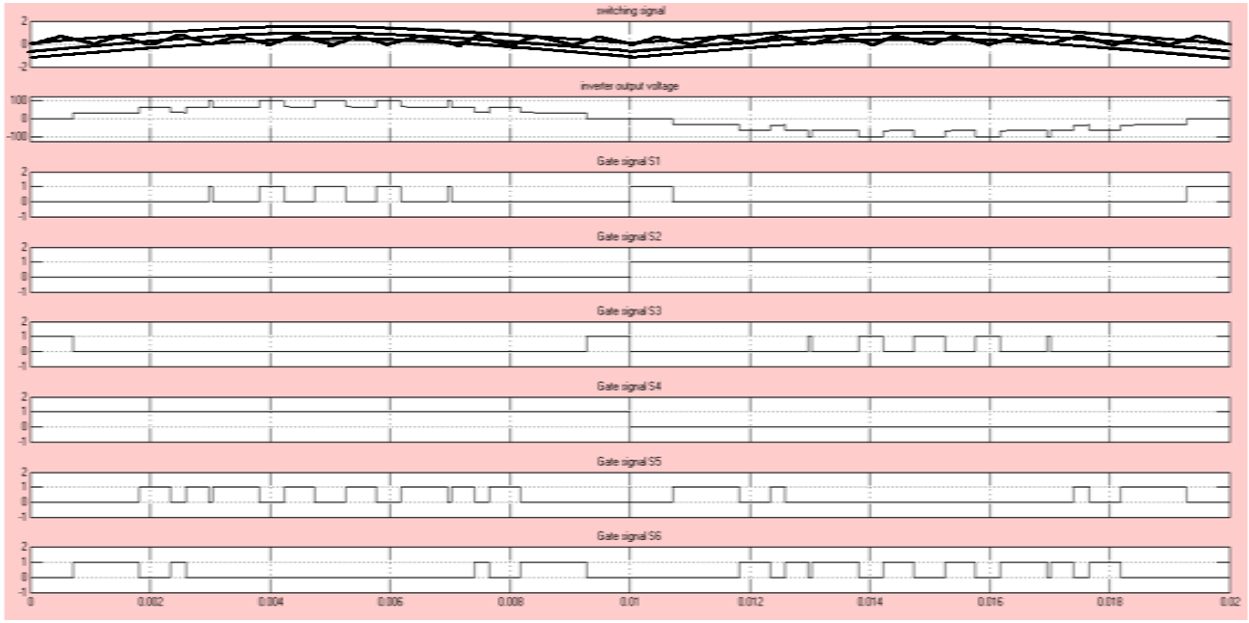
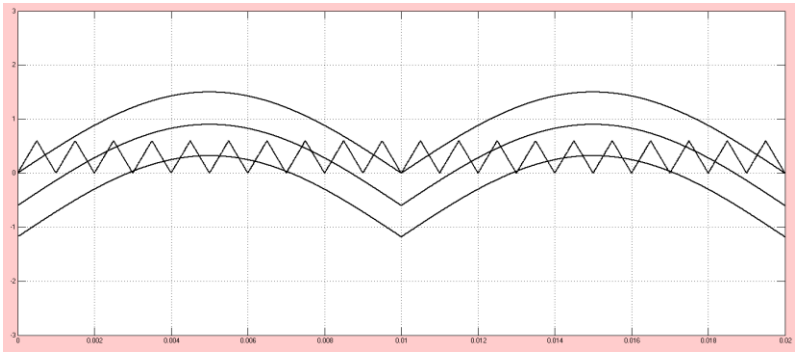
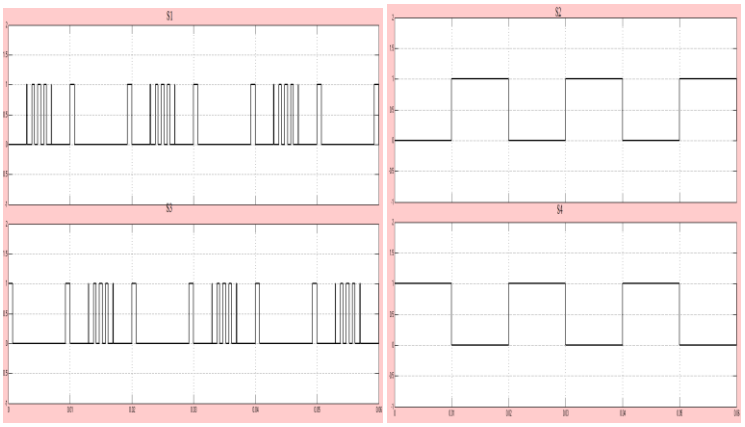


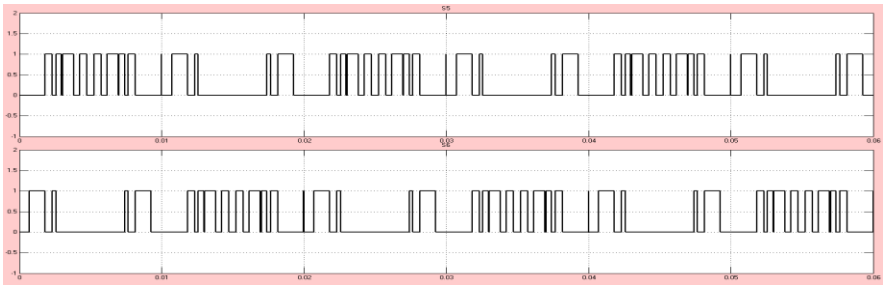
Figure 5 Switching pulse generation for the single-phase seven level inverter



(a) Single carrier and three sinusoidal reference signal



(b) PWM signals for S1 and S3 (c) PWM signals for S2 and S4



(d) PWM signals for S5 and S6

Figure 6 Detail Switching Signal for the single-phase seven level inverter

Fig.5 and Fig.6. shows the switching pattern to control and produce seven level inverter output voltages. To generate the PWM signals for the switches of the inverter, a simple PWM modulation technique was developed. This simple PWM modulation scheme which utilizes multi sinusoidal reference signal has fundamental frequency with single triangular carrier signal of high frequency. Three sinusoidal reference signals (V_{ref1}, V_{ref2}, and V_{ref3}) were compared with the carrier signal. If the amplitude of V_{ref1} has exceeded the peak amplitude value of $V_{carrier}$, then the amplitude of V_{ref2} was compared with $V_{carrier}$ until the reference signal amplitude had exceeded the peak amplitude of $V_{carrier}$. Then the amplitude of V_{ref3} would be compared with carrier signal until it reached zero. Once V_{ref3} had attained zero, V_{ref2} would be compared with $V_{carrier}$ until it reached zero. Then the amplitude of V_{ref1} would be compared with the carrier signal.. Switches S_1, S_3, S_5 and S_6 would be conducting at the rate of frequency of the carrier signal, whereas S_2 and S_4 would operate at equivalent to the fundamental frequency. The modified inverter operated into six conducting modes for one cycle of the fundamental frequency.

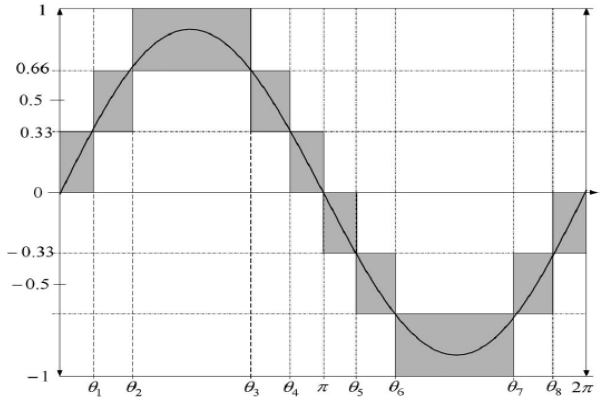


Figure 7 Output voltage and switching angles for seven level inverter

The conducting modes are expressed as follows:

Mode 1: $0 < \omega t < \theta_1$ and $\theta_4 < \omega t < \pi$

Mode 2: $\theta_1 < \omega t < \theta_2$ and $\theta_3 < \omega t < \theta_4$

Mode 3: $\theta_2 < \omega t < \theta_3$

Mode 4: $\pi < \omega t < \theta_5$ and $\theta_8 < \omega t < 2\pi$

Mode 5: $\theta_5 < \omega t < \theta_6$ and $\theta_7 < \omega t < \theta_8$

Mode 6: $\theta_6 < \omega t < \theta_7$.

The phase angle value varies with modulation index M_a. Theoretically, the modulation index for a single reference signal and a single carrier signal is defined to be $M_a = A_m / A_c$. Whereas the modulation index for a single-reference signal and a dual carrier signal is defined to be $M_a = A_m / 2A_c$, since the proposed seven level PWM inverter utilizes single-reference signal and three carrier signal is defined to be $M_a = Am / 3A_c$. where Ac represents the peak-to-peak value of carrier signal and Am represents the peak value of voltage reference signal Vref. The phase angle displacement for the modulation index value is less than 0.33 is defined to be $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \pi /2$; $\theta_5 = \theta_6 = \theta_7 = \theta_8 = 3\pi /2$. Since the phase angle displacement for the modulation index value is between 0.33 and 0.66 is defined to be $\theta_1 = \sin^{-1} (A_c/A_m)$; $\theta_2 = \theta_3 = \pi/2$; $\theta_4 = \pi-\theta_1$; $\theta_5 = \pi+\theta_1$; $\theta_6 = \theta_7 = 3\pi/2$; $\theta_8 = 2\pi-\theta_1$.If the modulation index value is more than 0.66, the phase angle displacement is $\theta_1 = \sin^{-1} (A_c/A_m)$; $\theta_1 = \sin^{-1} (2A_c/A_m)$; $\theta_3 = \pi-\theta_2$; $\theta_5 = \pi+\theta_1$; $\theta_6 = \pi+\theta_1$; $\theta_7 = 2\pi-\theta_2$; $\theta_8 = 2\pi-\theta_1$.Only the lower reference signal (V_{ref3}) is compared with the triangular carrier signal for Ma value that is equal to, or less than 0.33. The inverter's performance is like that of the conventional full-bridge three-level PWM inverter. However, only the Vref2 and Vref3 reference signals are compared with the triangular carrier signal for Ma value is between 0.33 and 0.66. The output voltage consists of five dc-voltage levels. The seven level output voltage to be produced for the modulation index value is more than 0.66. Three sinusoidal reference signals have to be compared with the single triangular carrier signal to produce the switching signals for control the switches of the inverter.

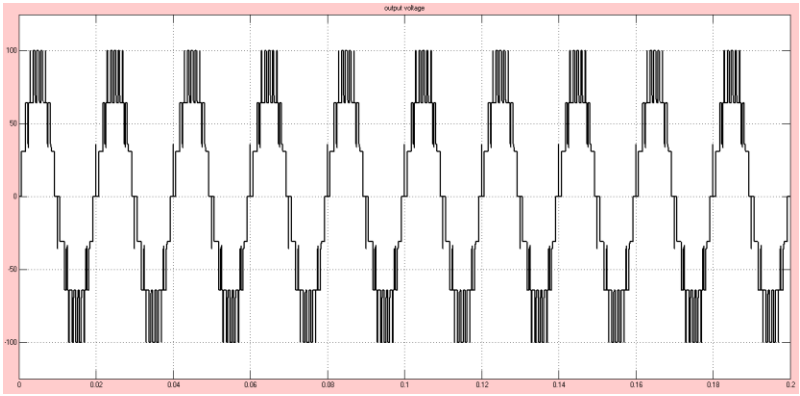


Figure 8 Output voltage for seven level inverter

The simulation result of inverter output voltage (V_{inv}) for seven-level inverter is shown in Fig.8. The inverter output voltage consists of seven levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$). The output voltage of the inverter can be controlled by varying the modulation index of the inverter. The level of the output voltage changes with range of modulation index, which is discussed earlier.

3. FIVE LEVEL MULTILEVEL INVERTER TOPOLOGY

The five level single-phase single dc sourced inverter is consists of single-phase conventional H-bridge inverter, one bidirectional switches and a capacitor voltage divider network of C_1, C_2. The H-bridge inverter topology has lot of advantageous over diode clamped and flying capacitor multilevel inverter topologies, it requires less number of components for inverters of the same number of levels and so its overall weight and price is also less. Photovoltaic arrays were connected to the multilevel inverter. The power generated by the multilevel inverter is to be delivered to the isolated load. Five output voltage levels can be produced by proposed switching of the multilevel inverter from the single dc supply voltage. The output voltage levels are V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$. The various levels of output voltage were generated as follows.

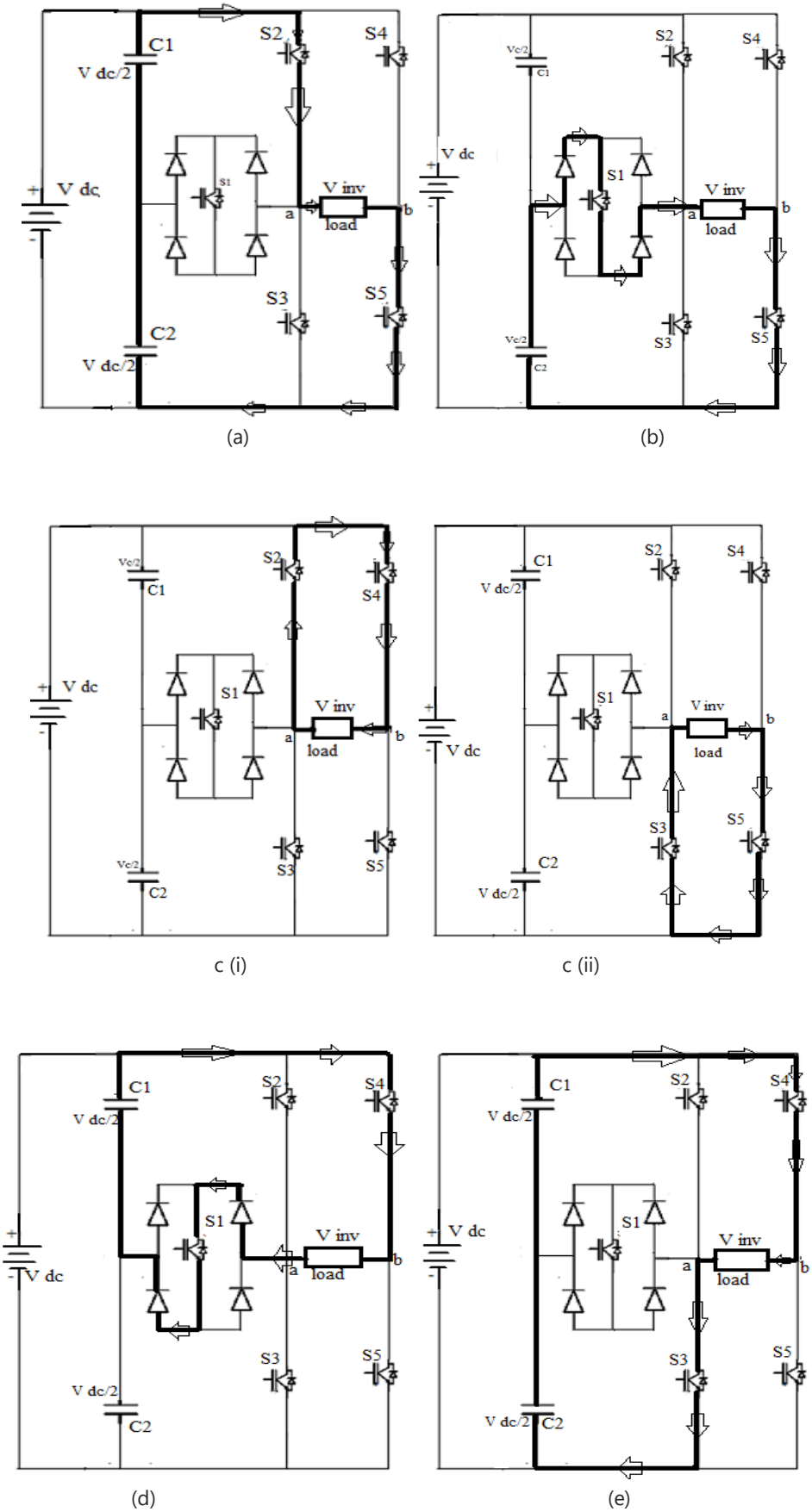


Figure 9 Switching combination required to generate the output voltage
(a) $V_{ab}=V_{dc}$ (b)$V_{ab}=V_{dc}/2$ c(i) and (ii) $V_{ab}= -V_{dc}/2$ (e)$V_{ab}= -V_{dc}$

Table 2 Output voltage according to the switches ON-OFF condition for five-level inverter

Inverter Output Voltage (Vo)	**Switching State Combination**				
	S_1	**S_2**	**S_3**	**S_4**	**S_5**
V_{dc}	0	1	0	0	1
$V_{dc}/2$	1	0	0	0	1
0	0	1	0	1	0
	0	0	1	0	1
$-V_{dc}/2$	1	0	0	1	0
$-V_{dc}$	0	0	1	1	0

Table 2 indicates the switching sequences that generated the five levels of output voltage (V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$).

Mode 1: (Maximum positive output voltage $+V_{dc}$)
In this mode, the switches S_2 and S_5 conducts. During this period, the current flows from switch S_2, load and S_5. When switch S_2 is ON, the load positive terminal connecting to V_{dc} and when switch S_5 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is $+V_{dc}$. Fig 11(a) shows the current path of this mode.

Mode 2: (Half positive output voltage ($+V_{dc}$ /2))
In this mode, the bidirectional switch S_1 and S_5 conducts. During this period, the current flows from bidirectional switch S_1, load and switch S_5. When the bidirectional switch S_1 is ON, the load positive terminal connecting to V_{dc} and when switch S_5 is ON, the load negative terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is ($+V_{dc}$ /2). Fig11 (b) shows the current path of this mode.

Mode 3: (Zero output voltage $0V_{dc}$)
This mode voltage can be produced by two combinations of switching; In this mode, the switches S_2 and S_3 conducts or S_4 and S_5 conducts, and the remaining switches are in OFF condition; the load terminal (a and b) is short circuit, the voltage between the load terminal is zero.Fig.11c(i) and (ii) shows the current path of this mode.

Mode 4: (Half negative output voltage ($-V_{dc}$ /2))
In this mode, the bidirectional switch S_1 and S_4 conducts. During this period, the current flows from bidirectional switch S_1, load and switch S_4. When the bidirectional switch S_1 is ON, the load positive terminal and when switch S_4 is ON, the load negative terminal connecting to V_{dc}. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is ($-V_{dc}$ /2). Fig 11(d) shows the current path of this mode.

Mode 5: (Maximum negative output voltage $-V_{dc}$)
In this mode, the switches S_3 and S_4 conducts. During this period, the current flows from switch S_3, load and S_4. When switch S_3 is ON, the load negative terminal connecting to V_{dc} and when switch S_4 is ON, the load positive terminal connecting to ground. Only two switches are conduct at the time. The remaining switches are in OFF condition; the voltage between the load terminal (a and b) is $-V_{dc}$. Fig11(e) shows the current path of this mode.

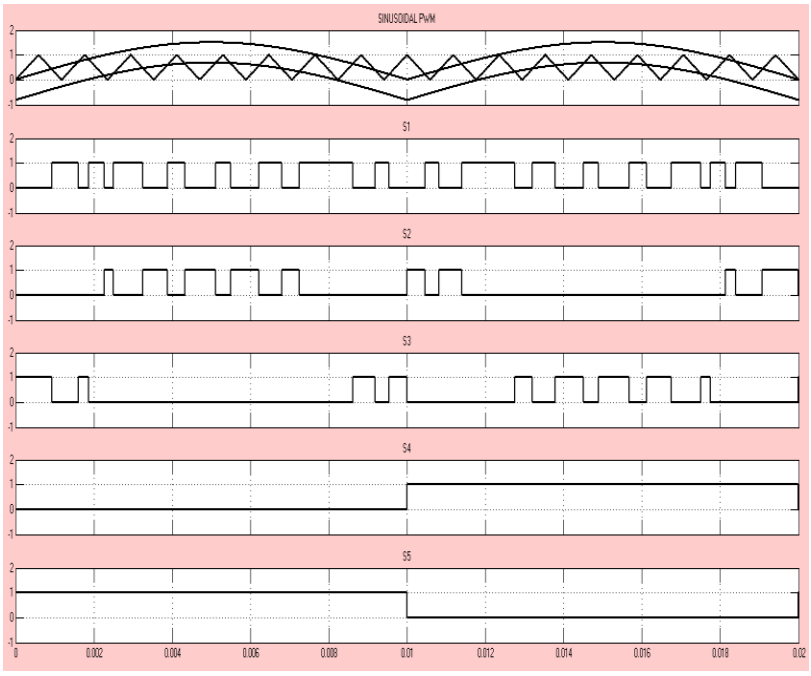
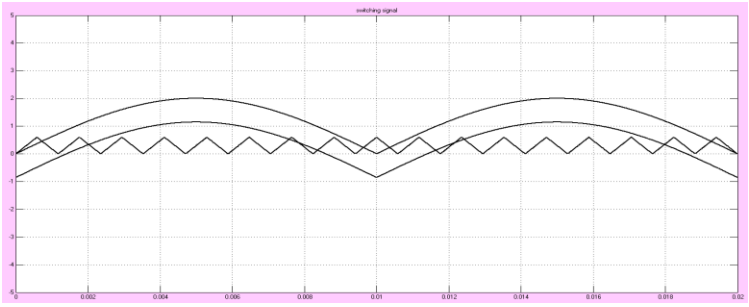
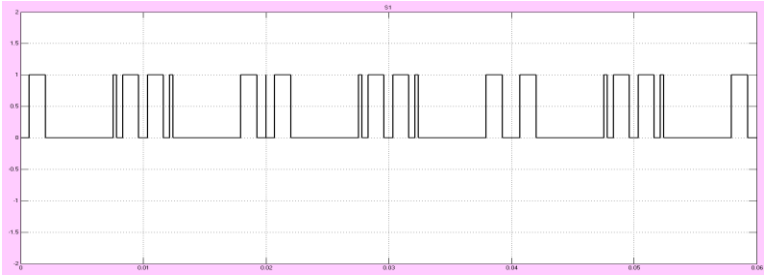


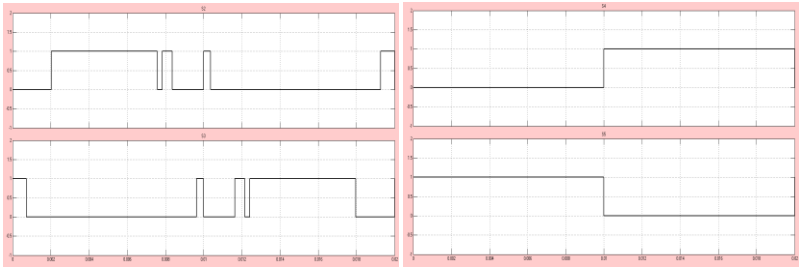
Figure 10 Switching pulse generation for the single-phase five level inverter



(a) Single carrier and two sinusoidal reference signal



(b) PWM signal for S_1



(c) PWM signals for S_2 and S_3 (d) PWM signals for S_4 and S_5

Figure 11 Detail switching signal for the single-phase five-level inverter

As Fig (10) shows that PWM signal generation for single-phase five-level inverter. Two sinusoidal reference signals and single triangular carrier signal have been used to achieve the five- level inverter output voltage. By comparing reference signal with carrier signal, switching signals are generated to control the switches of the multilevel inverter. Fig 11 (b),(c),(d) shows the switching signals for the controlled switches S_1 to S_5.

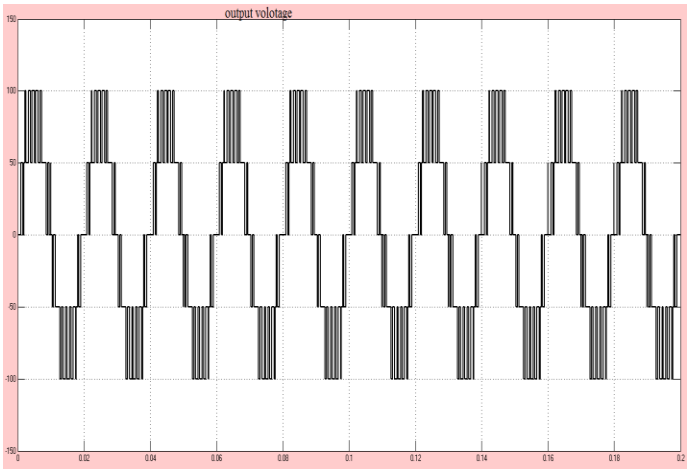


Figure 12 Output voltage for single-phase five-level inverter

The simulation result of inverter output voltage (V_{inv}) for five level inverter is shown in fig.12. The inverter output voltage consists of five levels (V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$).

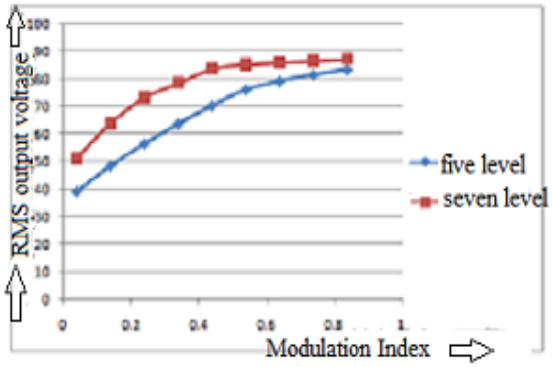


Figure 13 Comparison of modulation index and RMS output voltage

Fig.13 shows the graphical representation of comparison between Modulation index and RMS output voltage. From this representation, the value of RMS output voltage of seven level inverter is higher than the single-phase five-level inverter. So that, seven level inverter provides better performance.

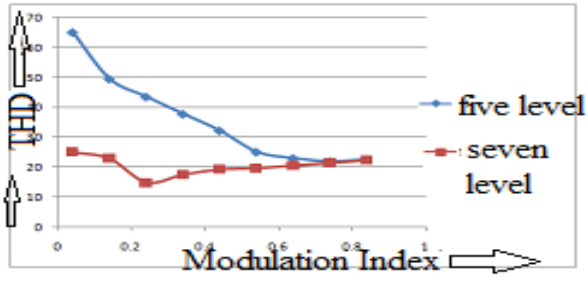


Figure 14 Comparison of Modulation index and THD

Fig.14 shows the graphical representation of comparison between Modulation index and Total Harmonics Distortion (THD) value. From this representation, the THD value of seven level inverter is decreased as compared to the five level inverter for the same value of Modulation index.

4. CONCLUSION

This paper carried out comparative studies on different level inverters for stand-alone Photovoltaic system for isolated applications. A simple PWM switching scheme has been developed and implemented for the five and seven level inverter. From this simulation studies, it is inform that, the performance of single-phase single DC sourced switched capacitored seven-level inverter provides improved THD with high value of fundamental rms output voltage for various values of modulation index. It is conclude that, the seven level inverter is an attractive solution for stand-alone PV inverters.

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